

a1  
7. (Amended) A processor according to Claim 1, wherein substantially all the second timing signal references are identical.

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11. (Amended) A digital video interface in accordance with Claim 9 in which the timing reference signals are identical.

12. (Amended) A digital video interface in accordance with Claim 9 in which there is no explicit F, V and H information in the timing reference signals.

a2  
13. (Amended) A digital video interface in accordance with Claim 9 in which aspect ratio information is carried in the timing reference signals.

14. (Amended) A digital video interface in accordance with Claim 9 in which line standard information is carried in the timing reference signals.

15. (Amended) A digital video interface in accordance with Claim 9 in which the timing reference signals include data identifying a method of scrambling.

16. (Amended) A digital video interface in accordance with Claim 9 in which the order of significance of the bits is rearranged.

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a3  
18. (Amended) A digital video interface in which data words are scrambled by a process which substitutes alternative data words for input data words in a manner known only to authorised recipients of the video, characterised in that specific words are prevented from being transmitted by re-submitting them to the scrambling process repeatedly until a valid word is obtained.

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a4  
20. (Amended) A digital video interface in accordance with Claim 19 in which valid unscrambled words are replaced by the corresponding input words to the unscrambling process.

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Please cancel Claim 22.